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Name: Combination: CSIT 3rd semester

Section: A Roll No: Subject: Computer Architecture

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| SN | Title | Date | Signature |
| 1. | Familiarizing with the syntax, data types, and operators of VHDL. | 2081/01/08 |  |
| 2. | Design of Basic Logic Gates using VHDL | 2081/01/08 |  |
| 3. | Design of Half Adder and Full Adder using VHDL | 2081/01/08 |  |
| 4. | Design of Multiplexer and De multiplexer using VHDL | 2081/01/08 |  |
| 5. | Design 4-bit binary-to-gray and gray-to-binary code converters using VHDL | 2081/01/09 |  |
| 6. | Design 8-bit parity generator and checker circuits using VHDL | 2081/01/09 |  |
| 7. | Design Encoder and Decoder using VHDL | 2081/01/09 |  |
| 8. | Design 2’s Complement Adder-Subtractor using VHDL | 2081/01/09 |  |
| 9. | Design of Registers using VHDL (SR flip-flop or JK flip-flop or D flip-flop or T flip-flop) | 2081/01/10 |  |
| 10. | Design 4-bit ALU using VHDL | 2081/01/10 |  |
| 11. | Design of CPU using VHDL | 2081/01/10 |  |
| 12. | Simulation of 5 stage or 4 stage or 3 stage pipelining | 2081/01/11 |  |
| 13. | Simulation of Booth addition and subtraction of signed 2’s complement data. ( Implement using VHDL or C ) | 2081/01/11 |  |
| 14. | Simulation of Boot multiplication and division algorithm. (Implement using VHDL or C program) | 2081/01/11 |  |